Atomic Layer Deposition for Next Generation CMOS Devices

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Outline:

• The high-k InGaAs (100) system- problems and possible solutions

• A quick guide to InGaAs (100) surfaces

• Atomic Layer Deposition for interface control and tailored surface engineering

• Interface control layers to partially overcome $D_{IT}$ issues

• Substrate cleaning prior to growth- optimised $(\text{NH}_4)_2\text{S}$ treatment

• In-situ substrate cleaning prior to growth using $(\text{NH}_4)_2\text{S}$

• Optical studies of ALD chemistry on InGaAs

• Conclusions, Outlook, Acknowledgements
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Motivation: beyond 2015

III-V MOSFETs for future CMOS:

- High-K gate
- High electron mobility Channel: e.g. high In % InGaAs
- High hole mobility Channel: Ge

<table>
<thead>
<tr>
<th>Material</th>
<th>Si (cm²/Vs)</th>
<th>Ge (cm²/Vs)</th>
<th>GaAs (cm²/Vs)</th>
<th>In₀.₅₃Ga₀.₄₇As (cm²/Vs)</th>
<th>InAs (cm²/Vs)</th>
<th>InSb (cm²/Vs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electron Mobility</td>
<td>1400</td>
<td>3900</td>
<td>8500</td>
<td>14000</td>
<td>40000</td>
<td>78000</td>
</tr>
<tr>
<td>Hole mobility</td>
<td>450</td>
<td>1900</td>
<td>400</td>
<td>300</td>
<td>500</td>
<td>850</td>
</tr>
</tbody>
</table>

III-V n-FETs combined with Ge p-FETs

Improved performance/power consumption ratio
Why use III-V channel materials in transistors?

III-V Materials

<table>
<thead>
<tr>
<th>Material</th>
<th>Electron mobility $\mu$ [cm$^2$/Vs]</th>
<th>Hole mobility $\mu$ [cm$^2$/Vs]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>1,400</td>
<td>450</td>
</tr>
<tr>
<td>Ge</td>
<td>3,900</td>
<td>1,900</td>
</tr>
<tr>
<td>InP</td>
<td>5,400</td>
<td>200</td>
</tr>
<tr>
<td>GaAs</td>
<td>8,500</td>
<td>400</td>
</tr>
<tr>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>14,000</td>
<td>350</td>
</tr>
<tr>
<td>InAs</td>
<td>40,000</td>
<td>500</td>
</tr>
<tr>
<td>InSb</td>
<td>77,000</td>
<td>850</td>
</tr>
</tbody>
</table>

High $\mu$  \iff  Higher Performance / Same Power

Same Performance / Lower Power
Why $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ Alloy Composition?

$\chi_{\text{HfO}_2} \sim 2.0 \text{ eV}$

$\Delta E_v \text{GaAs} \sim 2\text{eV}$

Defect(s) Energy Range?

$\Delta E_v 2.2-2.3\text{eV} (~ \text{constant})$

$\text{HfO}_2 5.8\text{eV}$

Band alignment studies using internal photoemission and photoconductivity

Lattice matched to InP for MOVPE growth

Other alloys have electrically active defects aligned in energy terms within the gap

If defects are outside of gap then they will not contribute to capacitance (but will still degrade mobility- interface is still a problem)

High-k on InGaAs- the problems

ALD of high dielectric constant oxides like HfO$_2$ on III-V substrates such as In$_{0.53}$Ga$_{0.47}$As leads to a poor interface.

Growth of In$_{0.53}$Ga$_{0.47}$As native oxides occurs regardless of the surface pretreatment and passivation method.

The presence of the native oxides leads to poor gate leakage current characteristics due to the low band gap of the native oxides and the presence of potential wells at the interface.

The poor quality of this interface leads to very large interface state defect densities, which are detrimental to metal-oxide-semiconductor-based device performance.

Possible solutions

- Use of interface control layers
- Better ex-situ substrate treatment
- **Better in-situ substrate treatment**
- Better post-growth treatments (e.g. forming gas anneal)

Monaghan et al., JVST B, 29, 1, 01A807, 2011
Abrupt ‘clean’ interfaces- to avoid Fermi level pinning and interface traps

Fermi Level Pinning: imperfections of various nature at semiconductor surfaces may cause pinning of the Fermi energy on the surface preventing changes of the surface potential in response to the changes of the voltage applied to the metal contact of metal-semiconductor and metal-insulator-semiconductor structures.

Interface traps: additional capacitance degrading device performance, reduction in mobility- where and what are these?

Channel, e.g. p-type InGaAs
In high-k?
In SC??
High-k, e.g. HfO$_2$
**Literature Analysis**


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**Diagram:**

- High-k layer
- Interlayer
- InGaAs

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Similar responses observed for various different high-k materials, with and without interlayers

**Conclude:** interface states arise at the InGaAs surface
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The nature of the interface states (on GaAs (100))

first-principles modeling of the HfO$_2$/GaAs strain-free interface

In-situ half-cycle ALD study of S-passivated GaAs showing (a) Ga 2p and (b) As 2p regions. The As-shaded feature corresponds to As-As bonding.

C.L. Hinkle et al., APL. 94 (2009) 162101.
Using GaAs as an example

(100) Surface - all Ga or all As
Bonding orientation alternates between orthogonal directions, layer to layer
Surface reconstructions:
Ga-Ga dimers align along \(<110>\)
As-As dimers align along \(<1-10>\)
Atomically clean InGaAs surfaces, from diffraction methods


A Gomyo et al., PRL, 72, (1994)


Atomically clean InGaAs surfaces, from diffraction and STM methods

(nx3) reconstructions - unique to the alloy

Atomically clean InGaAs surfaces, from diffraction and STM methods*

(a) RHEED patterns after the deposition of lattice matched In0.53Ga0.47As/InP showing a weak (4x3) surface reconstruction.

(b) 500 x 500 Ångstrom filled state STM image of this film.

(c) A higher magnification of the boxed region in (b) showing adjacent domains of the (6x4), with spacing 30a along the [11 0] and 40a along the [1 -1 0], and (4x3), with spacing 4a along the [11 0] and 3a along the [1 -1 0] surface reconstructions.

Atomically clean $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surfaces, from diffraction and STM/STS and DFT methods- Group III-rich (4x2)*

Undimerised In and Ga atoms in top layer

STS at 300 K - Fermi level resides between the valence band (VB) and mid-gap for n-type, and near the VB for p-type consistent with the surface being either pinned or having a large surface dipole.

DFT- strained unbuckled dimers responsible for pinning Group III surfaces likely to be less reactive towards oxygen than group V surfaces, during high-k oxide growth


Better interfaces with Group III termination?
Self-cleaning works better with Group III termination?
Hinkle et al., APL 94, 162101 2009
M. Passlack et al., APL. 68, 1099, 1996

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Key Enabling Technology for Infilling Colloidal Photonic Crystals

Atomic Layer Deposition (ALD)

Video animation of the ALD process

 Courtesy of Cambridge Nanotech Inc., USA
Experimental: ALD Reactors at Tyndall
200mm ALD Reactors at Tyndall

Dual chamber Cambridge Nanotech Fiji in the CFF
200mm ALD Reactors at Tyndall

Single chamber Cambridge Nanotech Fiji in the AMSG labs
Applied Materials Dual High-k/Metal Gate 300 mm ALD
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Interface Control Layers

Use ~1 nm of Al$_2$O$_3$ or MgO as interface control layers on III-V substrates, to:

- Minimise leakage current ($E_g \approx 8$ eV)
- Use HfO$_2$ ($\kappa \approx 20$) on ~1 nm Al$_2$O$_3$/MgO ($\kappa \approx 8-10$) for EOT scaling [1]
- Removal or reduction of native III-V oxides

With ICL

No ICL

III-V native oxide cleaning by ALD

- Self-cleaning of III-V native oxides (e.g. GaAs, InGaAs, InSb) reported by ALD of HfO$_2$ and Al$_2$O$_3$

- Removal of III-V native oxides leads to improved high-$\kappa$/III-V interface

→ Device performance improved


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Proposed removal of native oxides by Al$_2$O$_3$ and HfO$_2$

2 Al(CH$_3$)$_3$ + M$_2$O$_3$ → 2 M(CH$_3$)$_3$ + Al$_2$O$_3$  (M = In, Ga, As)


3 Hf(NCH$_3$C$_2$H$_5$)$_4$ + M$_2$O$_3$ → 4 M(NCH$_3$C$_2$H$_5$)$_3$ + 3 HfO$_2$
3 Hf(NCH$_3$C$_2$H$_5$)$_4$ + MO(OH) → M(NCH$_3$C$_2$H$_5$)$_3$ + HfO$_2$ + HNCH$_3$C$_2$H$_5$


S Klejna and S D Elliott, As$_4$ evolution +hydrocarbons, WODIM 2012
Experimental Details

Substrates

\[ n-\text{In}_{0.53}\text{Ga}_{0.47}\text{As}(2 \, \mu\text{m}, \text{Si}:\sim 3.5 \times 10^{17} \, \text{cm}^{-3})/\text{InP}(0.5 \, \mu\text{m}, \text{Si}:\sim 2 \times 10^{18} \, \text{cm}^{-3})/\text{InP} \]

ALD precursors

- \( \text{HfO}_2: \) Hf\((\text{N(C}_2\text{H}_5)(\text{CH}_3))_4)/\text{H}_2\text{O} \)
- \( \text{Al}_2\text{O}_3: \) Al\((\text{CH}_3)_3)/\text{H}_2\text{O} \)
- \( \text{MgO}: \) Cp\(_2\)Mg/\text{H}_2\text{O} \)

Deposition temperature: \( 250 \, ^\circ\text{C} \)

No wet \text{InGaAs} pre-treatment-test for self-cleaning action
Structural & electrical characterisation- no pre-treatment

- Al₂O₃ ICL devices show lowest leakage current density (2V)
- Highest leakage current for MgO ICL devices may be due to HfO₂-MgO mixing??
- Increasing leakage of Al₂O₃ ICL devices (3V) may be due to native oxides forming leakage pathways in untreated InGaAs
- Self-cleaning incomplete
- Evidence for reduction in $D_{IT}$ with Al₂O₃ ICL

O'Mahony et al., ECS Transactions, 33 (2) 69-82 (2010)
Detailed Interface Characterisation

Markus Boese, Yanhui Chen, Colm C. Faulkner, CRANN, Trinity College Dublin

No mixing is evident
Self-cleaning and interface control with 3-stage etch

Dramatic reduction in leakage current
Data consistent with thickness dependent tunnelling barrier

Monaghan et al., JVST B, 29, 1, 01A807, 2011
Self-cleaning and interface control with 3-stage etch

\[ p-\text{In}_{0.53}\text{Ga}_{0.47}\text{As}, \quad 5 \text{ nm HfO}_2, \quad \text{no ICL} \]

\[ p-\text{In}_{0.53}\text{Ga}_{0.47}\text{As}, \quad 5 \text{ nm HfO}_2, \quad 1 \text{ nm Al}_2\text{O}_3 \text{ ICL} \]

Left, without ICL, clear interface state defect response in the depletion region and marked contribution from interface states or border traps in the accumulation region (defective substrate)

Right, with ICL, dramatic reduction in interface states in depletion and much reduced dispersion in the accumulation region.

This is strong evidence that the inclusion of an Al$_2$O$_3$ ICL, even in the presence of a defective $p$-In$_{0.53}$Ga$_{0.47}$As layer, improves the quality of the interface

Monaghan et al., JVST B, 29, 1, 01A807, 2011
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**(NH₄)₂S optimisation- previous work**

Conclusions from XPS and AFM measurements: sample treated in 10% (NH₄)₂S for 20 min at room temperature with no surface pre treatment other than a standard de-greasing process to remove ambient carbon contamination, showed the best combination of results:

- low RMS roughness,
- low levels of As, In and Ga oxides as well as the largest As₂O contribution prior to annealing,
- possibly suggesting the largest contribution from sulphur surface bonds, which was reflected in the largest S 2p peak intensity.

Sample Preparation, \((\text{NH}_4)_2\text{S}\) Optimisation

- Degrease by sequentially rinsing for 1 min each in acetone, methanol, and isopropanol.

- \((\text{NH}_4)_2\text{S}\) concentrations of 22%, 10%, 5%, and 1% in deionized H2O, for 20 min, room temperature 295 K.

- Samples were introduced to the ALD chamber load lock base pressure of less than \(2 \times 10^{-8}\) mbar within 7 min after removal from the aqueous \((\text{NH}_4)_2\text{S}\) solution.

- \(\text{Al}_2\text{O}_3\) growth nominal thickness 8 nm, Cambridge Nanotech Fiji, TMA + water.

- Gate contacts 100 nm thick were formed by e-beam evaporation of Ni 60 nm, and Au 40 nm, through a shadow mask.

- Electrical tests were performed on capacitors of nominal 100 m diameter.

- the actual dimensions of the test devices were measured using an optical microscope for all samples. Multiple sites were examined in all cases to ensure the results are representative of device behavior.

- Larger and smaller device areas were measured on all samples and the capacitance scaled as expected with area.

O’Connor et al. J. Appl. Phys. 109, 024101 2011
Note the absence of any discernable roughness at the interface. This is important since this can give rise to scattering.
Variable Frequency C-V Analysis: n-type

NH$_4$S treated, Au/Ni / 8 nm Al$_2$O$_3$ / $n$-In$_{0.53}$Ga$_{0.47}$As/InP devices. Frequencies: 200 Hz, 400 Hz, 500 Hz, 800 Hz, 1 kHz, 1.5 kHz, 2.0 kHz, 2.5 kHz, 3.0 kHz, 4 kHz, 5 kHz, 8 kHz, 10 kHz, 20 kHz, 40 kHz, 80 kHz, and 100 kHz. The 1 kHz curves have been highlighted in red to illustrate that a more accurate representation of the interface defect response is obtained by measuring down to 200 Hz.

Further improvement?
E.g. forming gas anneal

O’Connor et al. J. Appl. Phys. 109, 024101, 2011
Variable Frequency C:V Analysis: p-type

NH$_4$S treated, Au/Ni / 8 nm Al$_2$O$_3$ / $p$-In$_{0.53}$Ga$_{0.47}$As/InP devices. Frequencies: 200 Hz, 400 Hz, 500 Hz, 800 Hz, 1 kHz, 1.5 kHz, 2.0 kHz, 2.5 kHz, 3.0 kHz, 4 kHz, 5 kHz, 8 kHz, 10 kHz, 20 kHz, 40 kHz, 80 kHz, and 100 kHz. The 1 kHz curves have been highlighted in red to illustrate that a more accurate representation of the interface defect response is obtained by measuring down to 200 Hz.

10% solution data now not noticeably better in terms of defect peak

But this procedure yields lowest dispersion and sharpest transition towards accumulation

Interface states manifest as additional capacitance on the inversion profile (true inversion is not achieved)

(constant capacitance determined by $C_{ox} +$ temp)
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In-situ substrate treatment, Mr John Mullins (poster)

Substrates: $n$-In$_{0.53}$Ga$_{0.47}$As (2 μm, $S: \sim 4.47 \times 10^{17}$ cm$^{-3}$)/InP(100)  
$p$-In$_{0.53}$Ga$_{0.47}$As (2 μm, Zn: $\sim 3.3 \times 10^{17}$ cm$^{-3}$)/InP(100)

Treatments: a) none  

b) 20 min; 10% ammonium sulphide ($\text{NH}_4\text{S}_2$) etch;  
$\sim$3 min transfer  
c) in situ exposure 50 x 50ms at 70°C

Dielectric: $\text{Al}_2\text{O}_3$ from TMA and water at 300°C

Device fabrication: 70nm Ni and 90nm Au, forming metal-oxide-semiconductor (MOS) capacitor gate stacks as found in MOSFET transistors
No pre-treatment: Au/Ni/Al₂O₃/n or p-doped In₀.₅₃Ga₀.₄₇As

Structural (TEM) and capacitance-voltage (CV) for control capacitors (left n-type, right, p-type) formed with no pre-treatment.

The CVs display large frequency dispersion, which is typical for non-optimised high-k/III-V MOS capacitors.
Ex-situ vs in-situ (NH$_4$)$_2$S treatment: Au/Ni/Al$_2$O$_3$/n-In$_{0.53}$Ga$_{0.47}$As

- **CV:** *in-situ* treated sample shows reduced negative voltage shift - reduction in fixed oxide charge near the interface.

- **IV:** *in-situ* treated sample shows reduced leakage current density - further indicating an improved high-$k$/III-V interface quality.
Ex-situ vs in-situ (NH₄)₂S treatment: Au/Ni/Al₂O₃/p-In₀.53Ga₀.47As

• CV: in-situ treated sample, reduced Dᵢₗ bump (circled) and less Dᵢₗ stretch-out, although the in-situ sample has increased frequency dispersion in accumulation, possibly due to increased border traps

• CV dispersion between the 1ˢᵗ and 2ⁿᵈ 1 kHz sweeps for the ex-situ sample suggests the presence of some permanent charge in deep traps near the oxide/III-V interface.

• IV: in-situ treated sample shows reduced leakage
Putting it all together: full MOSFET fabrication and test

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Reflectance anisotropy spectroscopy (RAS)

\[ \frac{\Delta r}{r} = \frac{r_{[\bar{1}10]} - r_{[110]}}{r_{[\bar{1}10]} + r_{[110]}}, \]

Studies of InGaAs surfaces using reflectance anisotropy spectroscopy (RAS)

We think that the (2 × 3) surface structure proposed by Gomyo et al. [8] shown in Fig. 4(a) is not consistent with our RDS results because it consists of the same number of dimers along [1 1 0] and [1 1 0]. The negative peak near 2.7 eV should be nearly zero if the surface has the same number of As-dimers in both orthogonal directions.

Feature assigned specifically to As-As dimers

Studies of InGaAs surfaces using reflectance anisotropy spectroscopy (RAS)

Further evidence for dimer assignment around 2.7 eV
Work on GaAs c(4x4) surfaces
As-As dimers aligned along <1-10>

Seeing changes at \((001)\) InGaAs surfaces during in-situ surface treatment using reflectance anisotropy spectroscopy (RAS)

In collaboration with Prof John McGilp, Trinity College Dublin

Ex-situ Studies of \((\mathrm{NH}_4)_2\mathrm{S}\) treatment of InGaAs (100)

In-situ studies of the ALD growth of \(\mathrm{Al}_2\mathrm{O}_3\) on InGaAs (100)

In-situ monitoring and atomic scale process control
Ex-situ detection of changes at InGaAs surfaces using Reflectance Anisotropy Spectroscopy (RAS)

RAS shows a large increase in surface anisotropy following \((\text{NH}_4)_2\text{S}\) treatment, consistent with dangling bond dimerisation along the \(<110>\) direction.

Mixture of As dimers, oxides, sulphides, sub-oxides?
In-situ detection of changes at InGaAs surfaces using Reflectance Anisotropy Spectroscopy (RAS)

2 nm Al$_2$O$_3$ in-situ

No exposure to precursors in ALD system

Al$_2$O$_3$ growth reduces surface anisotropy-consistent with breaking of dimers
Dimers or ordered oxides?

• Well-ordered oxidized InAs, InGaAs, InP, and InSb surfaces found by experiments.

• Epitaxial oxide-III-V interface insulating and free of defects related to the harmful Fermi-level pinning.

• Calculations: only O-III bonds involved in initial oxide formation due to the geometry of the III-V(100)c(8 × 2) substrate, which is responsible for the formation of the ordered interface.

• Target starting surface is therefore the c(8 × 2) - a surface, which enables the formation of stable adsorption sites with only nearest-neighbor indium atoms, and results in ordered oxide.

Temperature (and pretreatment?) therefore critical.

See this reconstruction with RAS?

M. P. J. Punkkinen et al., PHYSICAL REVIEW B 83, 195329, (2011)
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Conclusions and Outlook

Nanoscale surface chemistry has a massive impact on the nature of the electrical response from MOS devices based on InGaAs.

We can use ex-situ and now also in-situ surface treatments, while the ALD process itself also contributes to interface clean-up.

Efficacy of ALD self-clean depends upon the pretreatment and on substrate quality.

Best ex-situ pretreatment is ‘ammonium sulfide last’ with the optimum concentration around 10%.

In-situ ammonium sulfide appears promising alternative- redefine the process technologies for n-channel MOSFETS.

Need to aim for certain critical surface reconstructions?

RAS- a new way of looking at high-k on InGaAs processing on the atomic scale under ‘real’ conditions.
Acknowledgements

É. O'Connor¹, A. O'Mahony², B Brennan³, V Djara¹ V, K Cherkaoui¹, S Monaghan¹, R Nagle¹, S B Newcomb⁴, J Mullins¹, I M Povey¹, I R. Contreras⁵, M Milojevic⁶, G Hughes³, R M Wallace⁶ and P K Hurley¹

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Markus Boese, Yanhui Chen, Colm C. Faulkner, CRANN, Trinity College Dublin (TEM of ICLs)

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