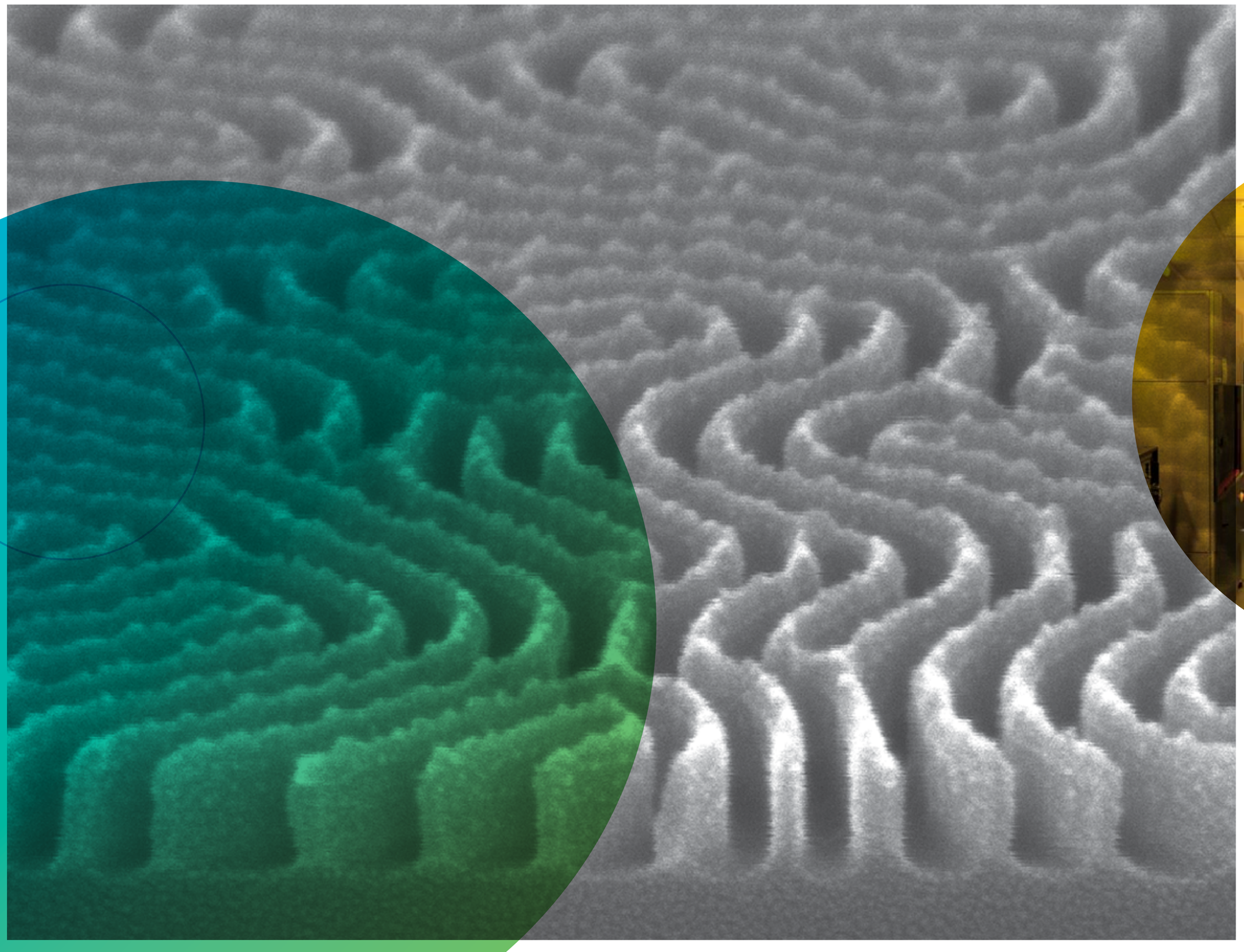
DELIVERING FOR INDUSTRY

INTEL

CRANN



INDUSTRY PROBLEM STATEMENT

The semiconductor roadmap, driven by Moore's Law, requires the density of semiconductor devices to double every 18 months. This drum beat of miniaturisation presents many challenges for transistors to halve in size through each new generation of technology.

A key challenge associated with the semiconductor roadmap is the requirement to develop new techniques for patterning the 300 mm silicon wafer controllably down to sub 20 nm dimensions.

CRANN VALUE ADD

CRANN has world leading experts and infrastructure in a diverse range of research areas, which when combined, has enabled significant breakthroughs in understanding and providing potential solutions to this challenge.

CRANN's material expertise enabled the utilisation of block copolymers to create scalable thin film templates at the required sub 20nm dimensions. The development of these materials required expertise in the pre and post processing of these materials via spin-coating techniques, thermal annealing and environmental control.

Using state-of the art cleanroom facilities and processes, the block-copolymer thin films were then preferentially etched to enable the creation of a nanometre dimension mask on silicon which was subsequently transferred directly to the silicon substrate. The silicon nanowires were characterised using scanning and transmission electron microscopy.

Advanced e-beam capability is enabling the contacting of these nanometre devices, which are being electrically tested to confirm performance and reliability.

This capability to use novel materials to pattern, create and contact nanometre scale devices is internationally leading and harnesses the unique infrastructure and capability at CRANN.

CRITICAL CRANN ENABLERS

- Nanomaterial processing and characterisation.
- Cleanroom facilities which enable controlled thin film lithography, etching and processing.
- E-beam lithography to contact sub 20nm devices and features.
- Scanning electron microscopy (SEM), scanning tunnelling microscopy (STM) and transmission electron microscopy (TEM) to image, contact and characterise nanowires and devices at the sub 20 nm dimension.
- Electrical contacting and testing of nanoscale devices.